SLLS057D – AUGUST 1989 – REVISED MARCH 1996

- **Capable of Running With All Existing TL16C450 Software**
- **After Reset, All Registers Are Identical to the TL16C450 Register Set**
- **In the FIFO Mode, Transmitter and Receiver Are Each Buffered With 16-Byte FIFOs to Reduce the Number of Interrupts to the CPU**
- **In the TL16C450 Mode, Holding and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data**
- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to (2^{16} – 1) and Generates an Internal 16× Clock**
- **Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream**
- **Independent Receiver Clock Input**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (dc to 256 Kbit/s)**
- **False-Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)**
- **Faster Plug-In Replacement for National Semiconductor NS16550A**

description

The TL16C550A is a functional upgrade of the TL16C450 asynchronous communications element (ACE). Functionally identical to the TL16C450 on power up (character mode†), the TL16C550A can be placed in an alternate mode (FIFO) to relieve the CPU of excessive software overhead.

In this mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two of the TL16C450 terminal functions (terminals 24 and 29 on the N package and terminals 27 and 32 on the FN package) have been changed to allow signalling of direct memory address (DMA) transfers.

The TL16C550A performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE's operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C550A ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to (2^{16} – 1) and producing a 16× clock for driving the internal transmitter logic. Provisions are included to use this 16× clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

† The TL16C550A can also be reset to the TL16C450 mode under software control.

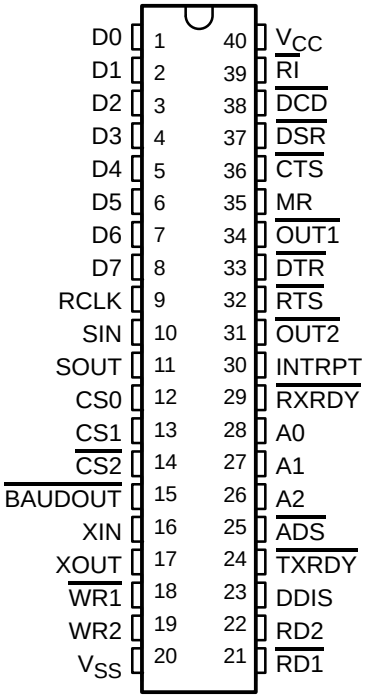


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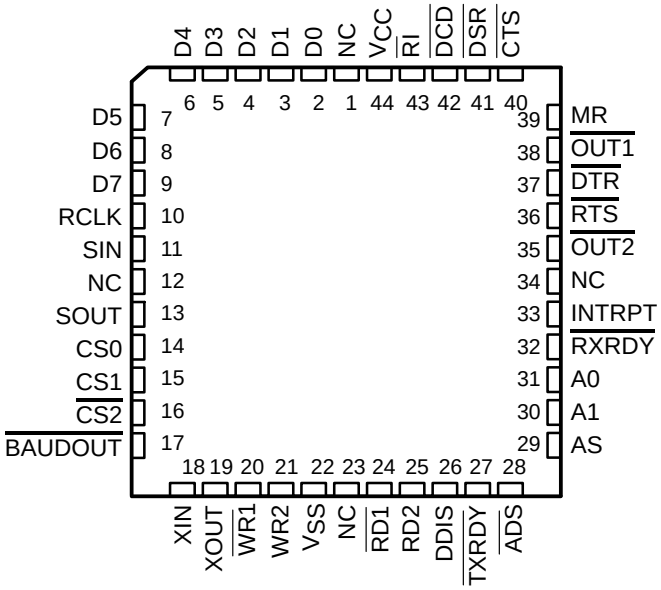
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N PACKAGE
(TOP VIEW)

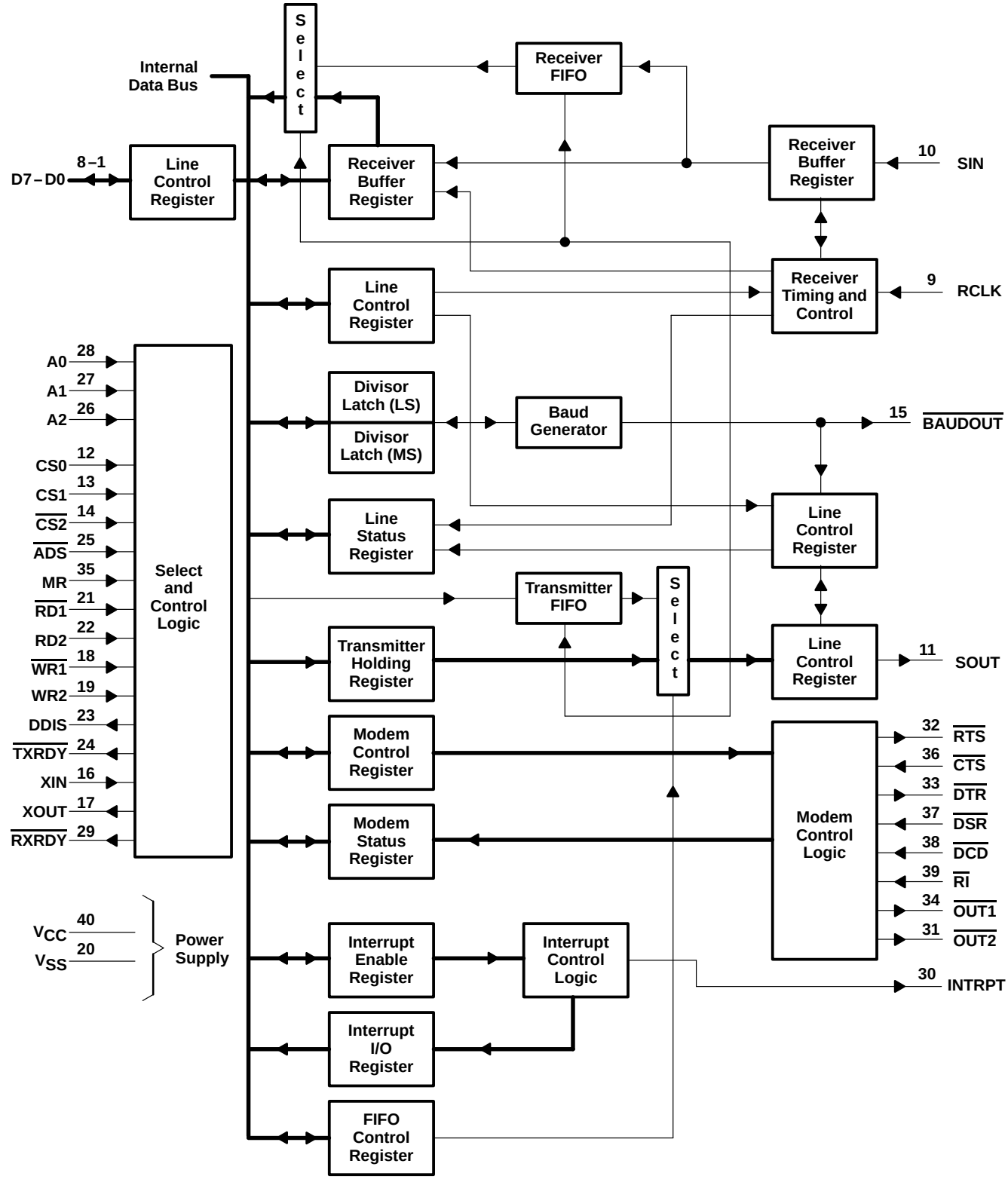


FN PACKAGE
(TOP VIEW)



NC – No internal connection

block diagram



NOTE A: Terminal numbers shown are for the N package.

Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
A0 A1 A2	28 [31] 27 [30] 26 [29]	I	Register select. A0, A1, and A2 are used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the address strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25 [28]	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the register select and chip select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15 [17]	O	Baud out. $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 $\overline{CS1}$ $\overline{CS2}$	12 [14] 13 [15] 14 [16]	I	Chip select. When CSx is active (high, high, and low respectively), the ACE is selected. If any of these inputs are inactive, the ACE remains inactive. Refer to the $\overline{ADS}$ (address strobe) signal description.
$\overline{CTS}$	36 [40]	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 – D7	1 – 8 [2 – 9]	I/O	Data bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38 [42]	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (DDCD) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23 [26]	O	Driver disable. This output is active (high) when the CPU is not reading data. When active, this output can disable an external transceiver.
$\overline{DSR}$	37 [41]	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33 [37]	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a master reset or during loop mode operation or clearing bit 0 (DTR) of the modem control register.
INTRPT	30 [33]	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available or timeout (FIFO mode only), transmitter holding register empty, or an enabled modem status interrupt. The INTRPT output is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35 [39]	I	Master reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{OUT1}$ $\overline{OUT2}$	34 [38] 31 [35]	O	Outputs 1 and 2. $\overline{OUT1}$ and $\overline{OUT2}$ are user-designated output terminals that are set to their active states by setting their respective modem control register bits (OUT1 and OUT2) high. $\overline{OUT1}$ and $\overline{OUT2}$ are set to their inactive (high) states as a result of master reset or during loop mode operations or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the modem control register.
RCLK	9 [10]	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.
$\overline{RD1}$ RD2	21 [24] 22 [25]	I	Read inputs. When either $\overline{RD1}$ or RD2 are active (high or low respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., RD2 tied low or $\overline{RD1}$ tied high).

† Terminal numbers shown in brackets are for the FN package.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
$\overline{RI}$	39 [43]	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32 [36]	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS modem control register bit, and is set to its inactive (high) state either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the modem control register.
$\overline{RXRDY}$	29 [32]	O	Receiver ready output. Receiver direct memory access (DMA) signalling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected with FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR0 = 0 or FCR0 = 1, FCR3 = 0), if there is at least 1 character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ is active (low). When RXRDY has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). In DMA mode 1 (FCR0 = 1, FCR3 = 1), when the trigger level or the timeout has been reached, $\overline{RXRDY}$ goes active (low); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (high).
SIN	10 [11]	I	Serial input. SIN is a serial data input from a connected communications device.
SOUT	11 [13]	O	Serial output. SOUT is a composite serial data output to a connected communication device. SOUT is set to the marking (high) state as a result of master reset.
$\overline{TXRDY}$	24 [27]	O	Transmitter ready output. Transmitter DMA signalling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected with FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40 [44]		5-V supply voltage
V_{SS}	20 [22]		Supply common
$\overline{WR1}$ WR2	18 [20] 19 [21]	I	Write inputs. When either $\overline{WR1}$ or WR2 are active (high or low respectively) while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	16 [18] 17 [19]	I/O	External clock. XIN and XOUT connect the ACE to the main timing reference (clock or crystal).

† Terminal numbers shown in brackets are for the FN package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range at any input, V_I . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	–0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = –1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kbit/s			10	mA
C_{XIN}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, All other terminals grounded, f = 1 MHz, T_A = 25°C		15	20	pF
C_{XOUT}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XOUT.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC		175		ns
t_{w5}	Pulse duration, $\overline{ADS}$ low	t_{ADS}	2, 3	15		ns
t_{w6}	Pulse duration, write strobe	t_{WR}	2	80		ns
t_{w7}	Pulse duration, read strobe	tRD	3	80		ns
t_{w8}	Pulse duration, master reset	t_{MR}		1		ns
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	t_{AS}	2, 3	15		ns
t_{su2}	Setup time, CS before $\overline{ADS}\uparrow$	t_{CS}	2, 3	15		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{DS}	2	15		ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	t_{AH}	2, 3	0		ns
t_{h2}	Hold time, CS valid after $\overline{ADS}\uparrow$	t_{CH}	2, 3	0		ns
t_{h3}	Hold time, CS valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WCS}	2	20		ns
t_{h4}§	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WA}	2	20		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{DH}	2	15		ns
t_{h6}	Hold time, CS valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RCS}	3	20		ns
t_{h7}§	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RA}	3	20		ns
t_{d4}§	Delay time, CS valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{CSW}	2	15		ns
t_{d5}§	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{AW}	2	15		ns
t_{d6}§	Delay time, write cycle, $\overline{WR1}\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	t_{WC}	2	80		ns
t_{d7}§	Delay time, CS valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{CSR}	3	15		ns
t_{d8}§	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{AR}	3	15		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	tRC	3	80		ns

§ Applicable only when $\overline{ADS}$ is tied low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	t_{XH}	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	t_{XL}	1	f = 9 MHz maximum	50		ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2$\uparrow$ to data valid	t_{RVD}	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to floating data	t_{HZ}	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Disable time, $\overline{RD1}\downarrow\uparrow$ or RD2$\uparrow\downarrow$ to DDIS$\uparrow\downarrow$	t_{RDD}	3	C_L = 100 pF		60	ns

NOTE 2: Charge and discharge time is determined by V_{OL}, V_{OH}, and external loading.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	t_{LW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	t_{HW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	100		ns
t_{d1}	Delay time, XIN$\uparrow$ to $\overline{BAUDOUT}\uparrow$	t_{BLD}	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, XIN$\uparrow\downarrow$ to $\overline{BAUDOUT}\downarrow$	t_{BHD}	1	C_L = 100 pF		125	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample clock	t_{SCD}	4			100	ns
t_{d13}	Delay time, stop to set RCV error interrupt or read RBR to LSI interrupt or stop to $\overline{\text{RXRDY}}\downarrow$	t_{SINT}	4,5,6,7,8			1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	t_{RINT}	4,5,6,7,8	C_L = 100 pF		150	ns

NOTE 3: In FIFO mode RC = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, INTRPT to transmit start	t_{IRS}	9		8	24	baudout cycles
t_{d16}	Delay time, start to interrupt	t_{STI}	9		8	8	baudout cycles
t_{d17}	Delay time, WR THR to reset interrupt	t_{HR}	9	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	t_{SI}	9		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	t_{IR}	9	C_L = 100 pF		140	ns
t_{d20}	Delay time, write to TXRDY inactive	t_{WXI}	10,11	C_L = 100 pF		195	ns
t_{d21}	Delay time, start to TXRDY active	t_{SXA}	10,11	C_L = 100 pF		8	baudout cycles

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d22}	Delay time, WR MCR to output	t_{MDO}	12	C_L = 100 pF		100	ns
t_{d23}	Delay time, modem interrupt to set interrupt	t_{SIM}	12	C_L = 100 pF		170	ns
t_{d24}	Delay time, RD MSR to reset interrupt	t_{RIM}	12	C_L = 100 pF		140	ns

PARAMETER MEASUREMENT INFORMATION

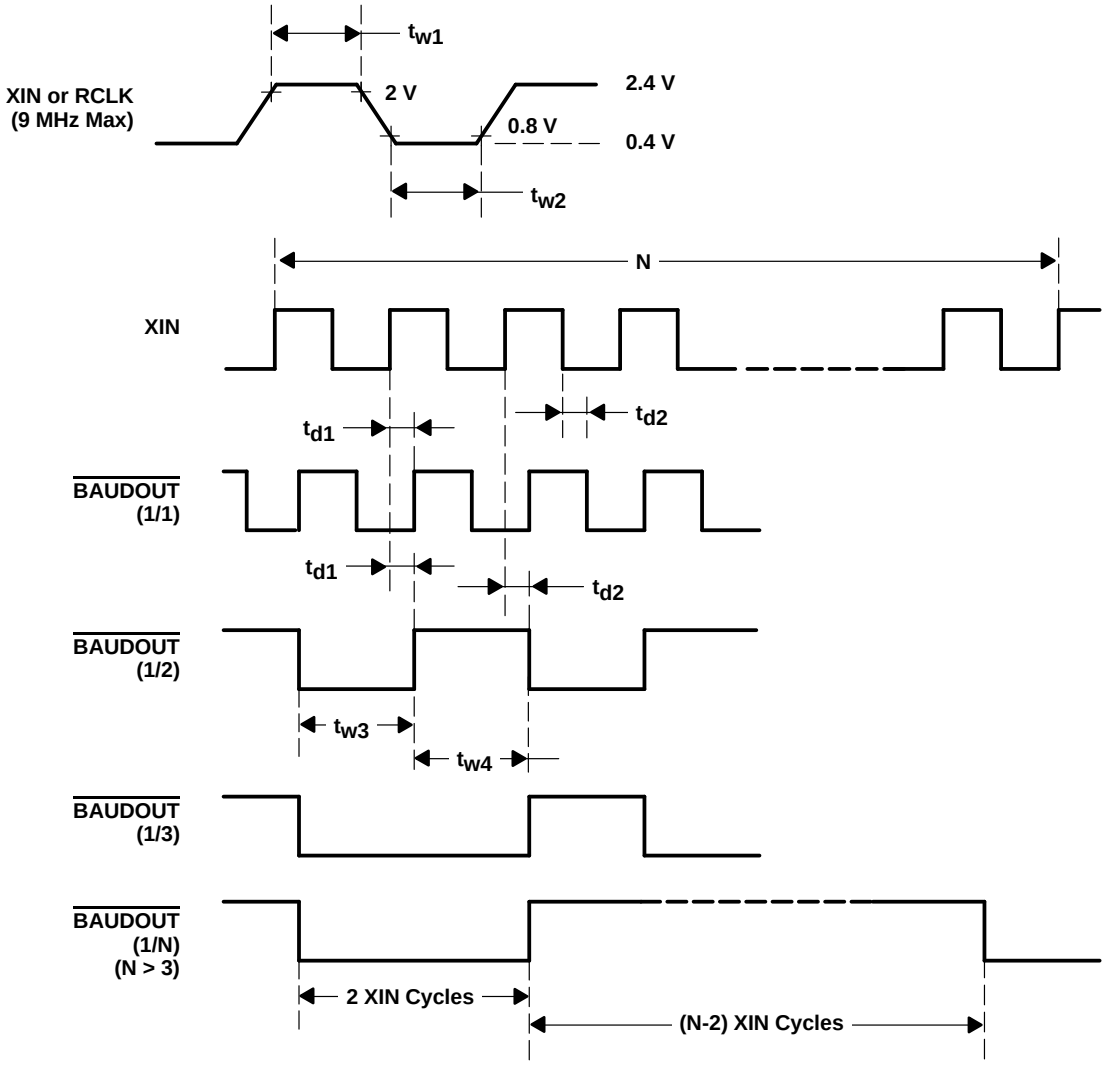
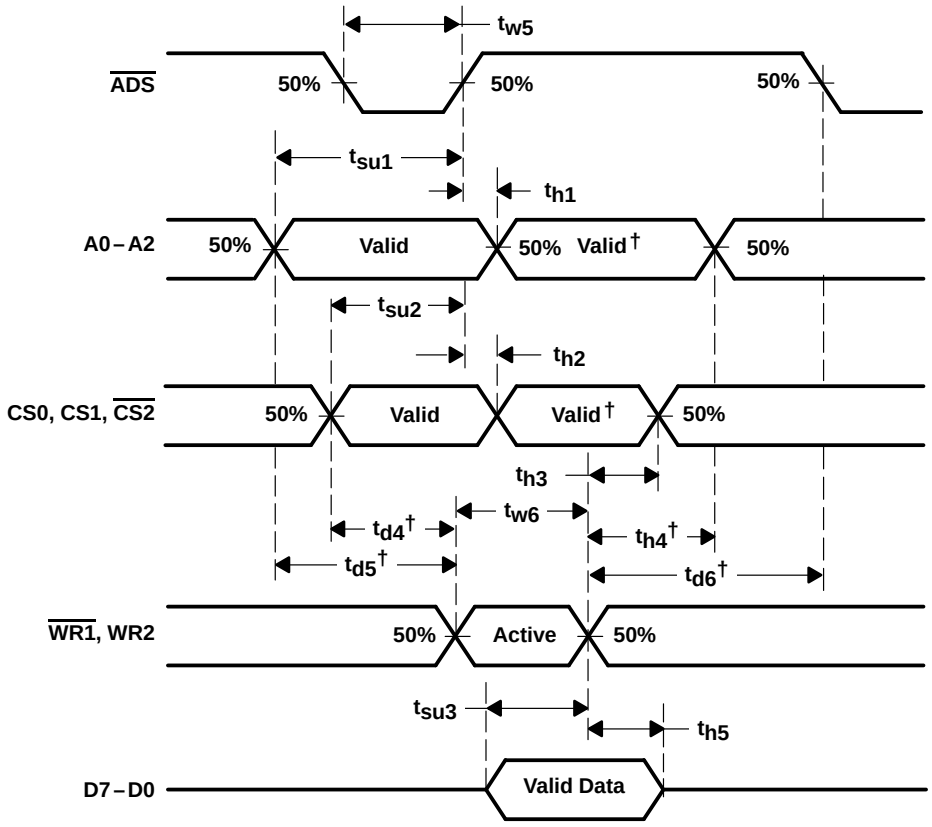


Figure 1. Baud Generator Timing Waveforms

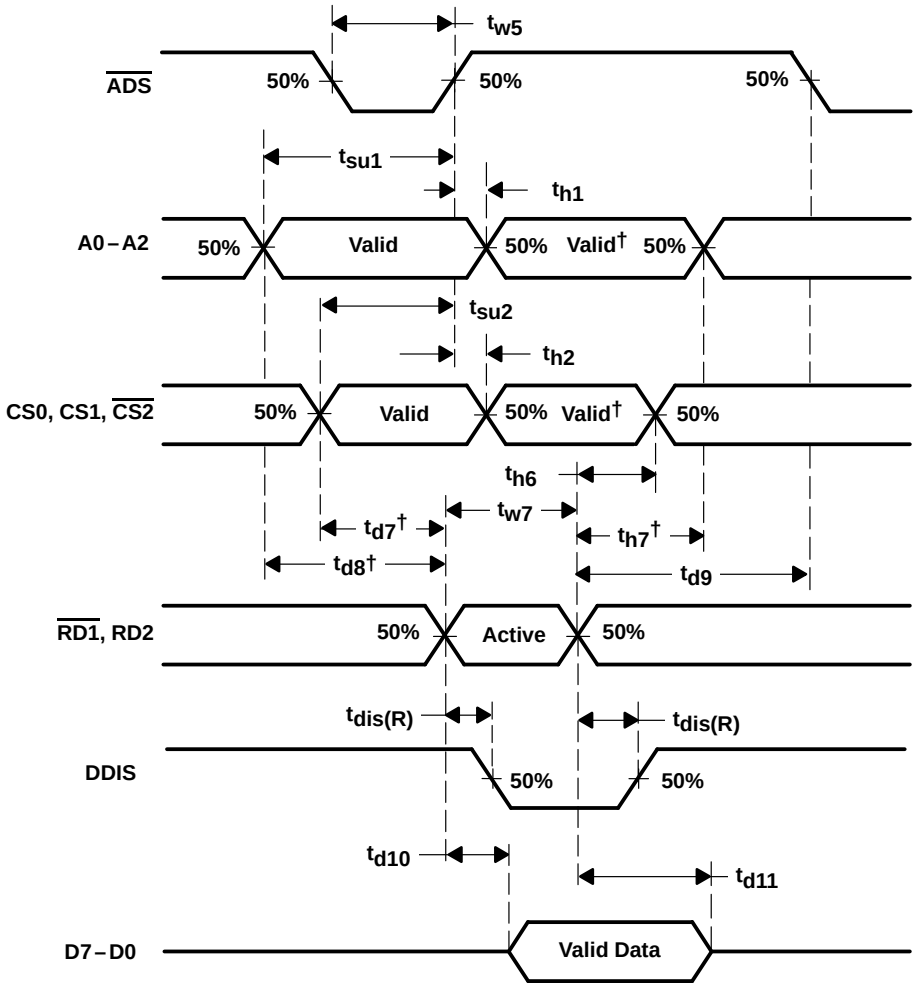
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

Figure 2. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{\text{ADS}}$ is tied low.

Figure 3. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

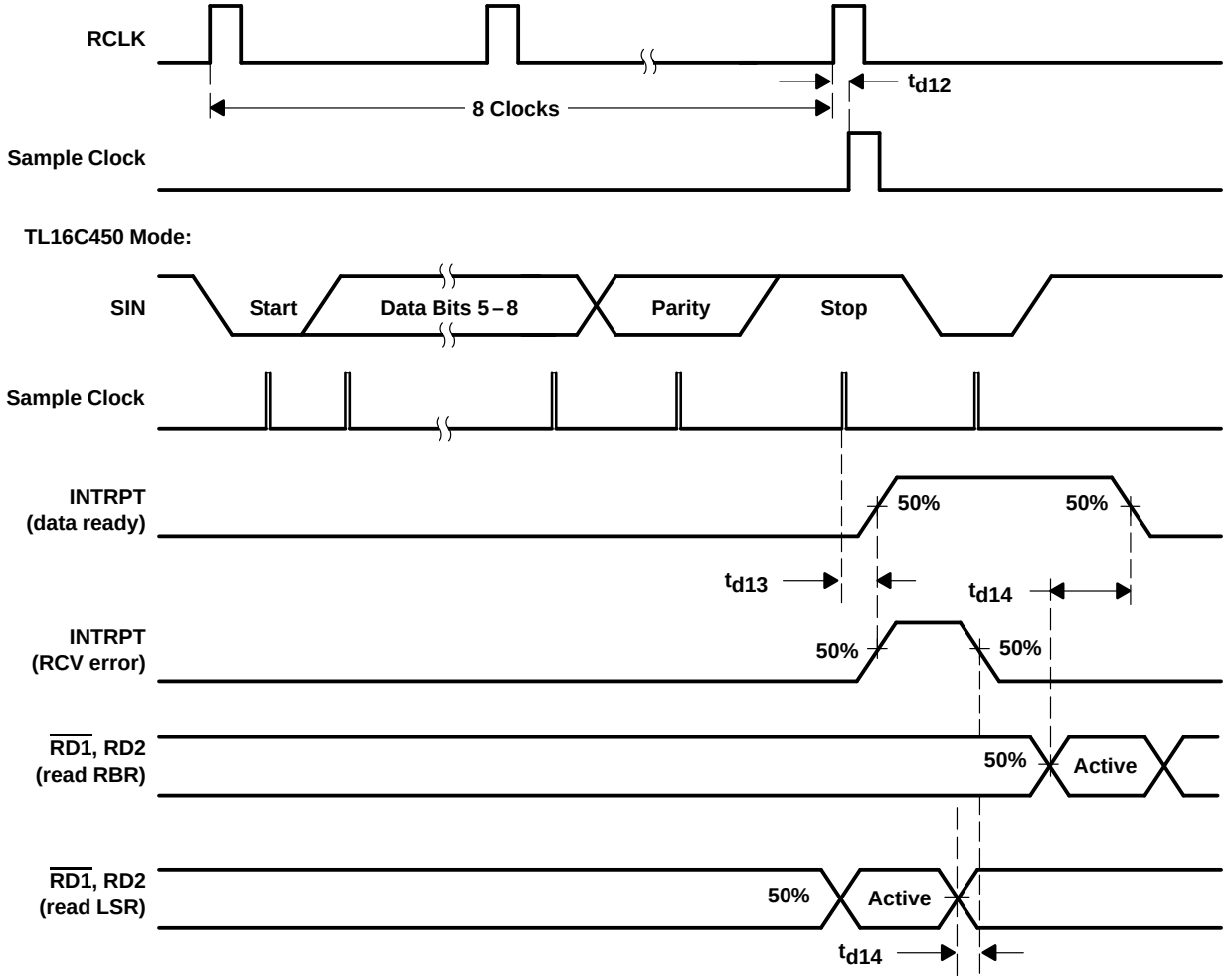
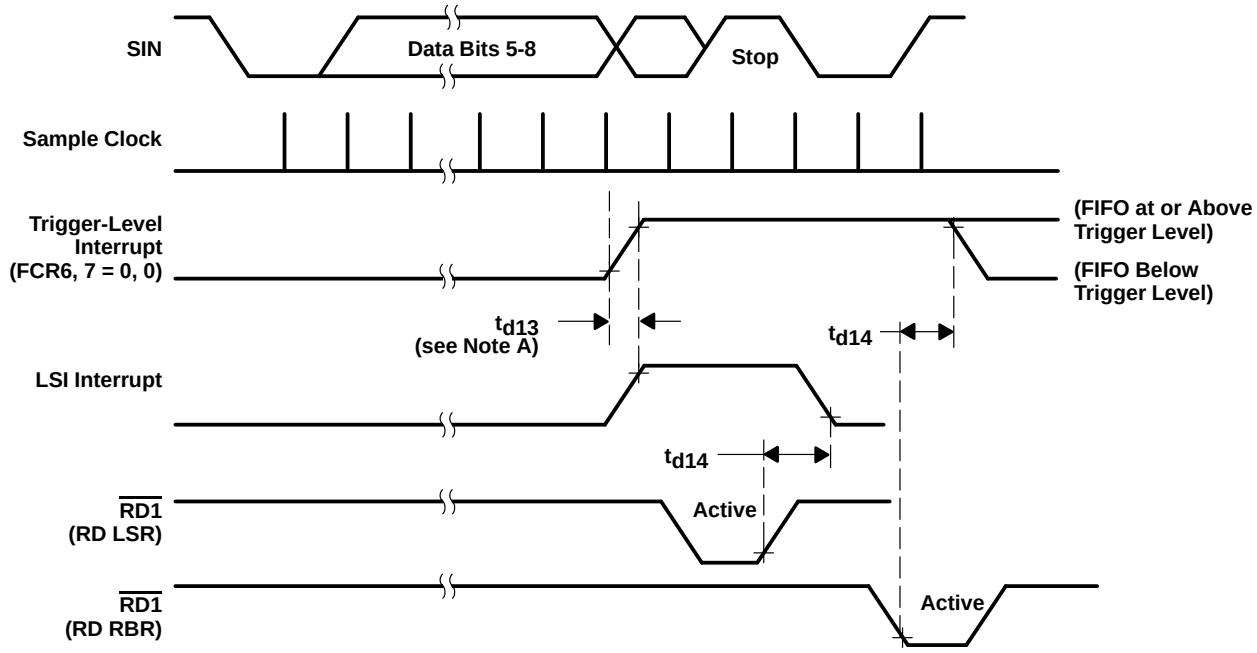


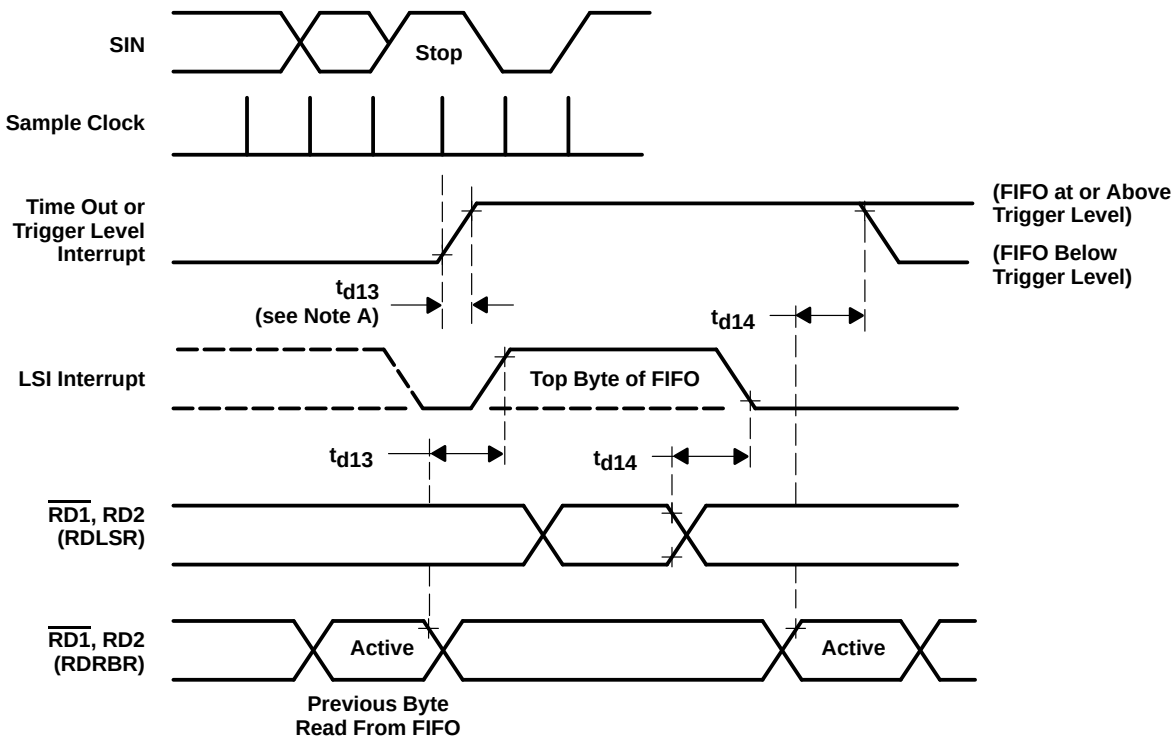
Figure 4. Receiver Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: For a timeout interrupt, t_{d13} = 8 RCLKs.

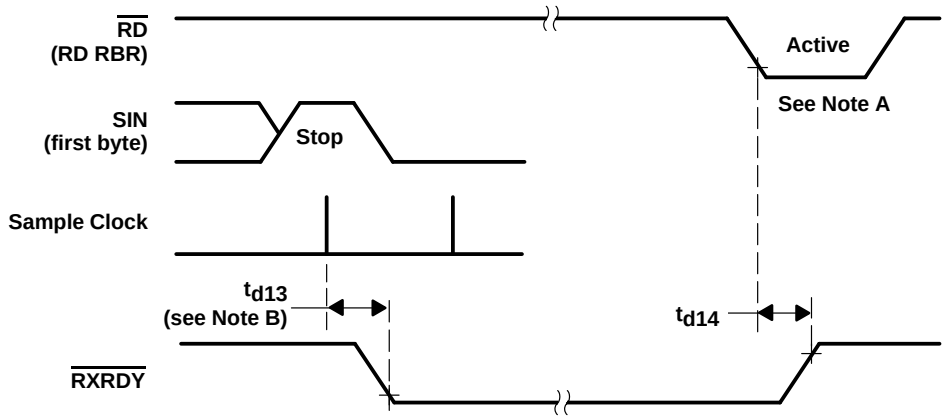
Figure 5. Receiver FIFO First Byte (Sets DR Bit) Waveforms



NOTE A: For a timeout interrupt, t_{d13} = 8 RCLKs.

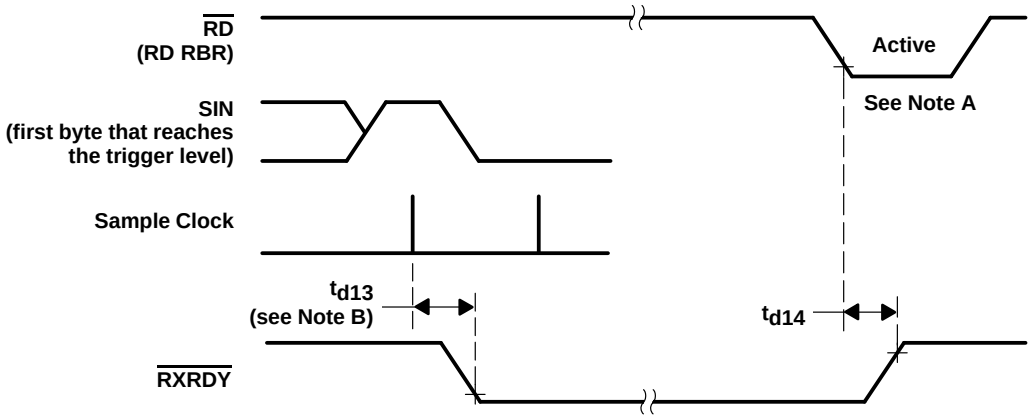
Figure 6. Receiver FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

Figure 7. Receiver Ready ($\overline{\text{RXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (mode 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

Figure 8. Receiver Ready ($\overline{\text{RXRDY}}$) Waveforms, FCR = 1 or FCR3 = 1 (mode 1)

PARAMETER MEASUREMENT INFORMATION

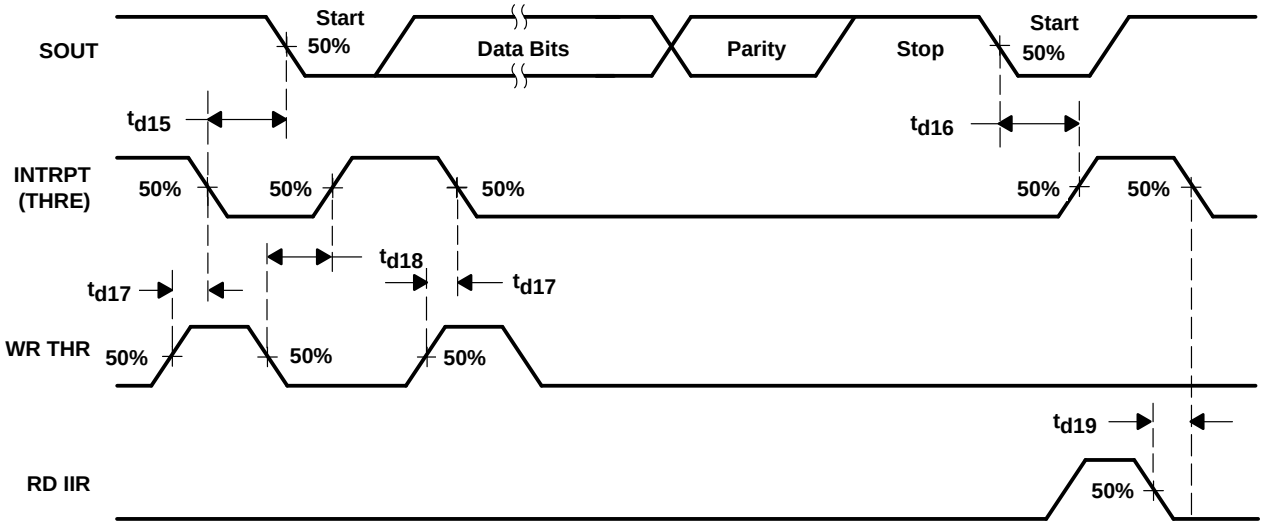


Figure 9. Transmitter Timing Waveforms

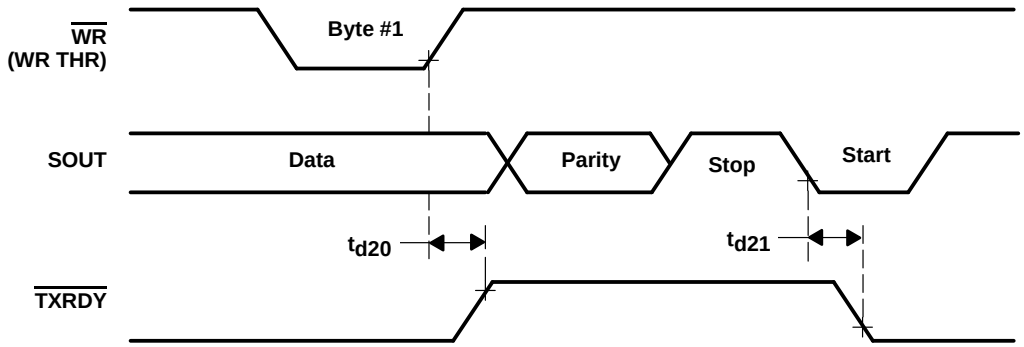


Figure 10. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (mode 0)

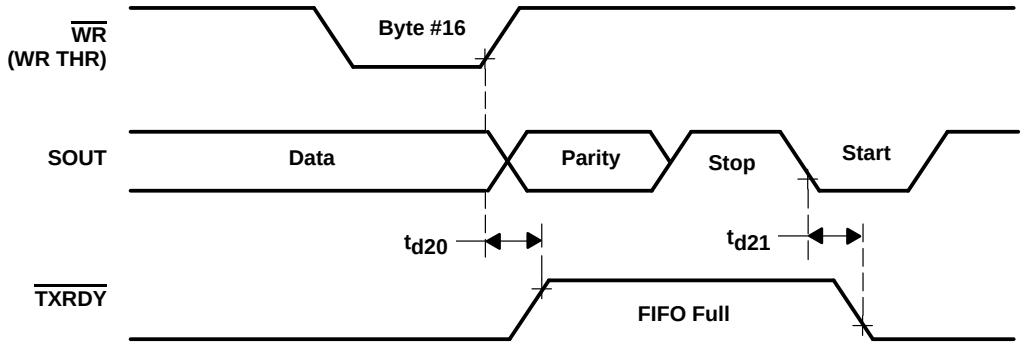


Figure 11. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 1 and FCR3 = 1 (mode 1)

PARAMETER MEASUREMENT INFORMATION

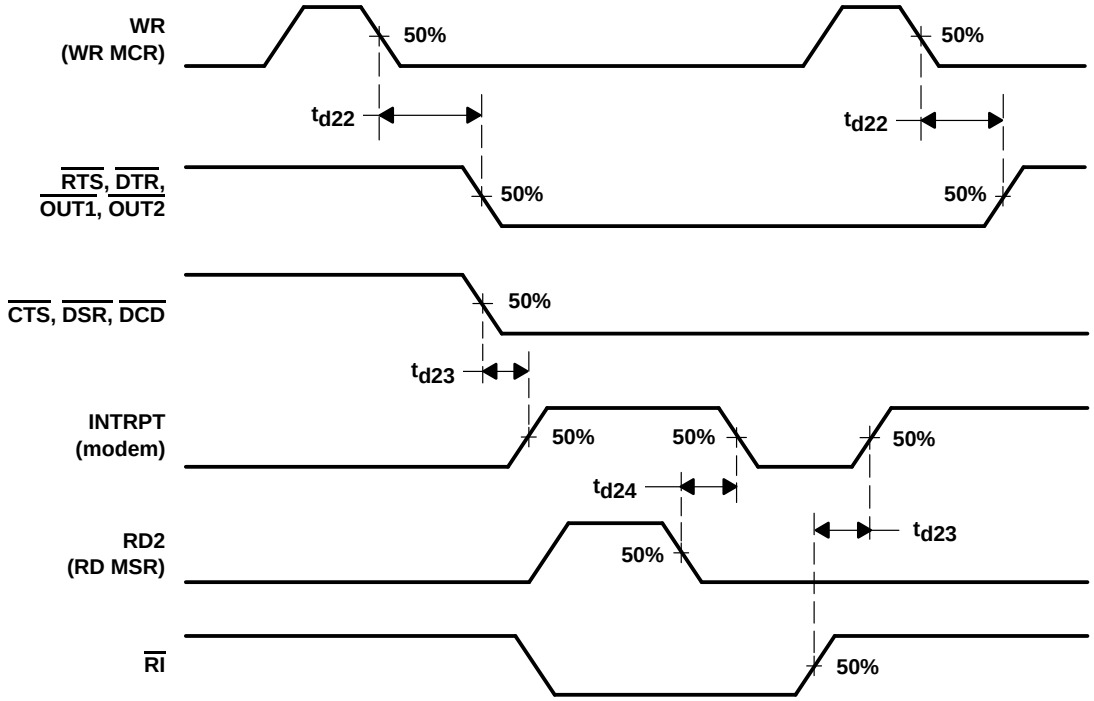


Figure 12. Modem Control Timing Waveforms

APPLICATION INFORMATION

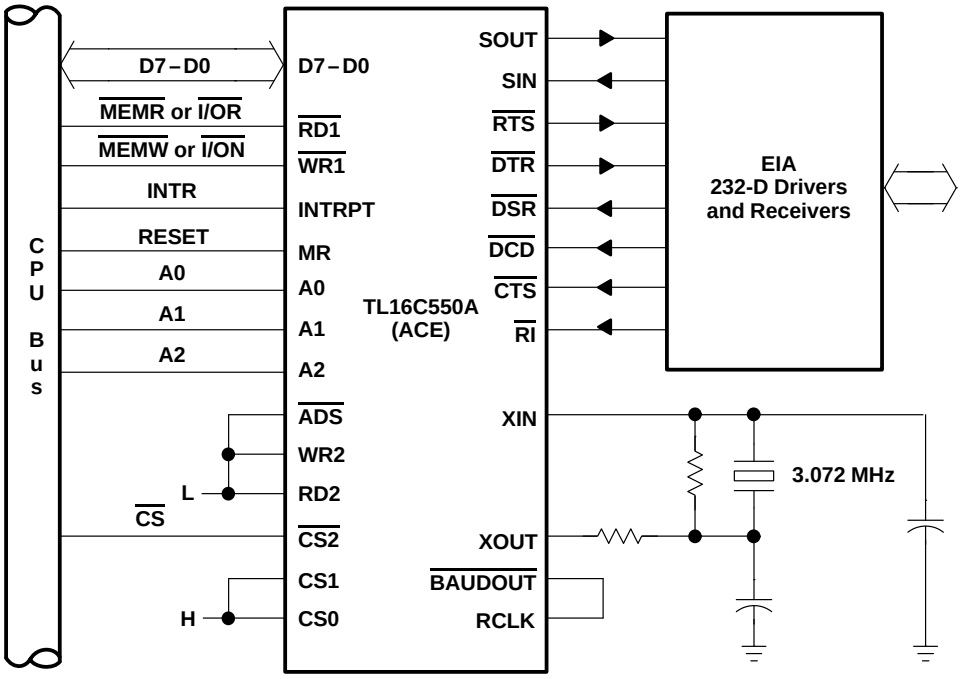


Figure 13. Basic TL16C550A Configuration

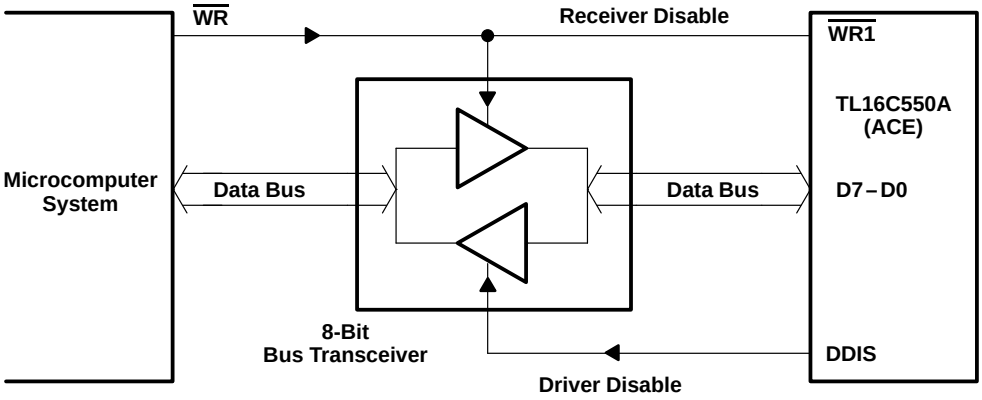
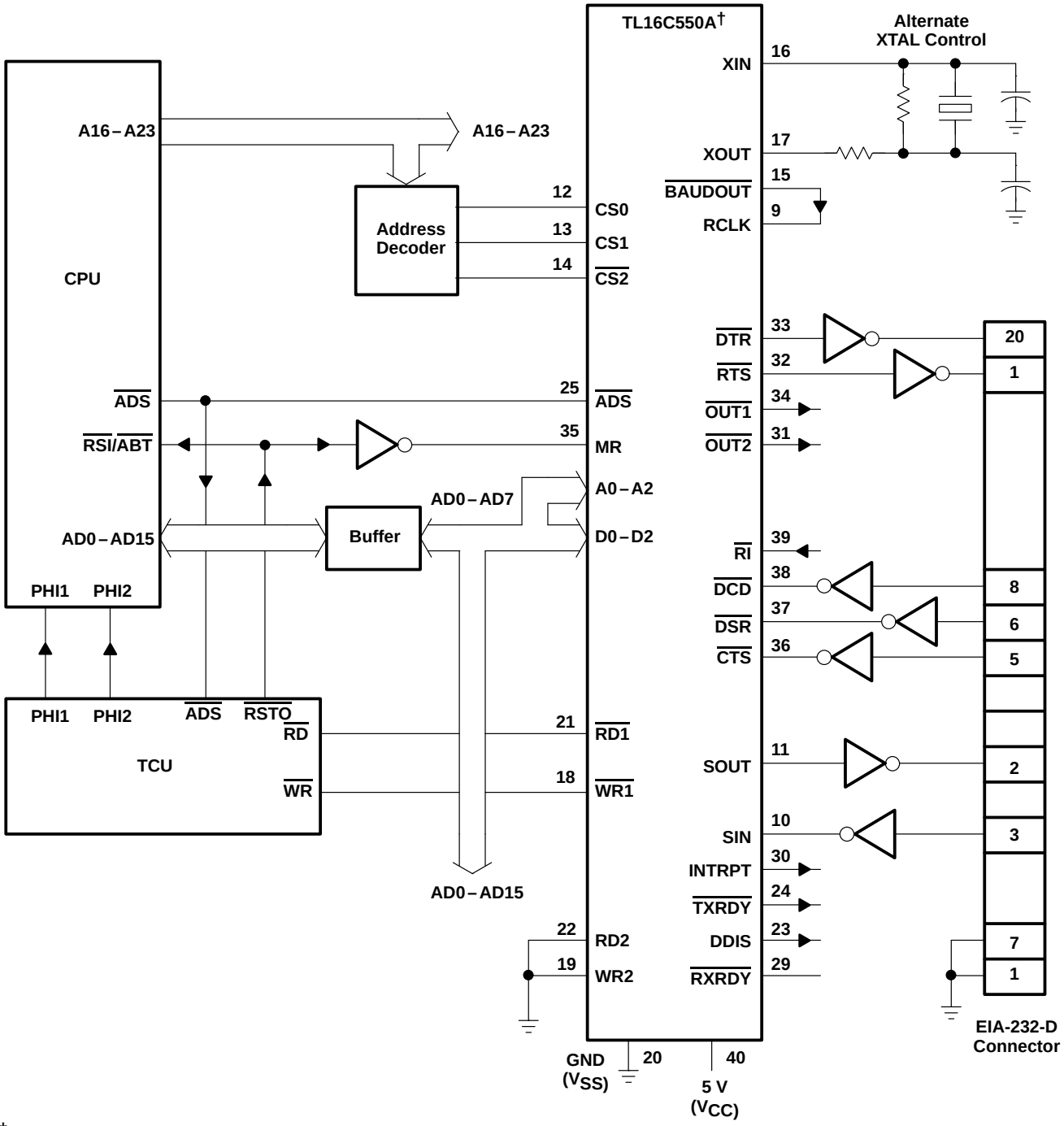


Figure 14. Typical Interface for a High-Capacity Data Bus

APPLICATION INFORMATION



† Terminal numbers for the TL16C550A are for the N package.

Figure 15. Typical TL16C550A Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is set, bits 1–3 are cleared, and bits 4–7 are permanently cleared
FIFO Control Register	Master Reset	All bits cleared
Line Control Register	Master Reset	All bits cleared
Modem Control Register	Master Reset	All bits cleared (5–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are set, all other bits are cleared
Modem Status Register	Master Reset	Bits 0–3 are cleared, bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT1}}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Registers	Master Reset	No effect
Transmitter Holding Registers	Master Reset	No effect
RCVR FIFO	MR/FCR1-FCR0/ ΔFCR0	All bits low
XMIT FIFO	MR/FCR2-FCR0/ ΔFCR0	All bits low

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERB)	”0“ If Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Transmitter FIFO Reset	Number of Stop Bits (STB)	Out1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 4)	DMA Mode Select	Parity Enable (PEN)	Out2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 4)	Receiver Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 4)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 4)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
NOTE 4: These bits are always cleared in the TL16C450 mode.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables the FIFOs, clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit (FCR0), when set, enables the transmit and receive FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit (FCR1), when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 2: This bit (FCR2), when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 3: When this bit (FCR0) and FCR3 are set, $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ change from mode 0 to mode 1.
- Bits 4 and 5: These two bits (FCR4 and FCR5) are reserved for future use.
- Bits 6 and 7: These two bits (FCR6 and FCR7) set the trigger level for the receiver FIFO interrupt. Table 4 shows the trigger level for the receiver FIFO interrupt.

Table 4. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) receiver interrupts occur as follows:

1. The receive data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared as soon as the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and, like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, receiver FIFO timeout interrupts occur as follows:

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. FIFO timeout interrupt occurs when the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character received was longer than 4 continuous character times ago (when 2 stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO was longer than 4 continuous character times ago. This causes a maximum character received to interrupt issued delay of 160 ms at 300 baud with 12-bit characters.
2. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
3. When a timeout interrupt has occurred, it is cleared and the timer reset when the microprocessor reads one character from the receiver FIFO.
4. When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The THR interrupt (02) occurs when the transmit FIFO is empty. It is cleared as soon as the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmit FIFO empty indications are delayed 1 character time minus the last stop bit time when the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, if it is enabled.

Character timeout interrupt and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt. The transmit FIFO empty interrupt has the same priority as the current THRE interrupt.

FIFO polled mode operation

When FCR0 is set, clearing IER0, IER1, IER2, IER3, or all four puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks the receiver and transmitter status using the LSR.

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 – LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode and the IIR is not affected since IER2 = 0.
- LSR5 indicates when the transmit FIFO is empty.
- LSR6 indicates that both the transmit FIFO and shift registers are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or timeout conditions indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

PRINCIPLES OF OPERATION

interrupt enable register (IER)

The IER enables each of the four types of interrupts (refer to Table 5) and the INTRPT output signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit, when set, enables the received data available interrupt.
- Bit 1: This bit, when set, enables the THRE interrupt.
- Bit 2: This bit, when set, enables the receiver line status interrupt.
- Bit 3: This bit, when set, enables the modem status interrupt.
- Bits 4 – 7: These bits in the IER are not used and are always cleared.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and the type of interrupt is defined by the interrupt's three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4. Details of each bit are as follows:

- Bit 0: This bit can be used either in a hardwire prioritized or polled interrupt system. When this bit is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: This bit is always cleared in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a timeout interrupt is pending.
- Bits 4 thru 5: These two bits are not used and are always cleared.
- Bits 6 and 7: These two bits are always cleared in the TL16C450 mode. They are set when bit 0 of the FCR is set.

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER (IIR)				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	–
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Reading the line status register (LSR)
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode.	Reading the receiver buffer register (RBR)
1	1	0	0	2	Character timeout indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time	Reading the receiver buffer register (RBR)
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (IIR) (if source of interrupt) or writing into the transmitter holding register (THR)
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register (MSR)

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 6.

Table 6. Serial Character Word Length

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks the first stop bit only, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in Table 7.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

Table 7. Number of Stop Bits Generated

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in the transmitted data between the last data word bit and the first stop bit. In received data, when bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1's in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. When bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition, i.e., a condition where the serial output (SOUT) terminal is forced to the spacing (low) state. When bit 6 is cleared, the break condition is disabled. The break condition has no affect on the transmitter logic; it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are described in the following bulleted list and summarized in Table 3.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. Bit 0 is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO and is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When bit 1 is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten but is not transferred to the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment
‡ Bits 1 through 4 are the error conditions that produce a receiver line status Interrupt.

PRINCIPLES OF OPERATION

line status register (LSR)† (continued)

- Bit 2‡: This bit is the parity error (PE) indicator. When bit 2 is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3‡: This bit is the framing error (FE) indicator. When bit 3 is set, it indicates that the received character did not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE then samples this start bit twice and then accepts the input data.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When bit 4 is set, it indicates that the received data input was held clear for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only the 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. Bit 5 is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, then an interrupt is generated. THRE is set when the contents of the THR are transferred to the transmitted shift register. This bit is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. Bit 6 is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, the TEMT bit is cleared. In the FIFO mode, this bit is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550A, this bit is always cleared. In the TL16C450 mode, this bit is cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the data terminal ready ($\overline{DTR}$) output. Setting bit 0 forces the $\overline{DTR}$ output to its low state. When bit 0 is cleared, $\overline{DTR}$ goes high.
- Bit 1: This bit (RTS) controls the request to send ($\overline{RTS}$) output in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 2: This bit (OUT1) controls the output 1 ($\overline{OUT1}$) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bit 3: This bit (OUT2) controls the output 2 ($\overline{OUT2}$) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When bit 4 is set, the following occurs:

  1. The SOUT is set high.
  2. The SIN is disconnected.
  3. The output of the TSR is looped back into the RSR input.
  4. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  5. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  6. The four modem control output terminals are forced to their inactive states (high).

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

- Bit 5 – 7: These bits are permanently cleared.

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear to send (ΔCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input has changed states since the last time it was read by the CPU . When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the compliment of the clear to send ($\overline{CTS}$) input. When bit 4 (loop) of the MCR is set, bit 4 is equivalent to the MCR bit 1 (RTS).
- Bit 5: This bit is the compliment of the data set ready ($\overline{DSR}$) input. When bit 4 (loop) of the MCR is set, bit 5 is equivalent to the MCR bit 1 (DTR).

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 6: This bit is the compliment of the ring indicator ($\overline{RI}$) input. When bit 4 (loop) of the MCR is set, bit 6 is equivalent to the MCR bit 2 (OUT1).
- Bit 7: This bit is the compliment of the data carrier detect ($\overline{DCD}$) input. When bit 4 (loop) of the MCR is set, bit 7 is equivalent to the MCR bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 8 MHz and divides it by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16× the baud rate. The formula for the divisor is:

divisor # = XIN frequency input ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 8 and 9, which follow, illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively For baud rates of 38.4 kbit/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 16 for examples of typical clock circuits.

Table 8. Baud Rates Using a 1.8432-MHz Crystal

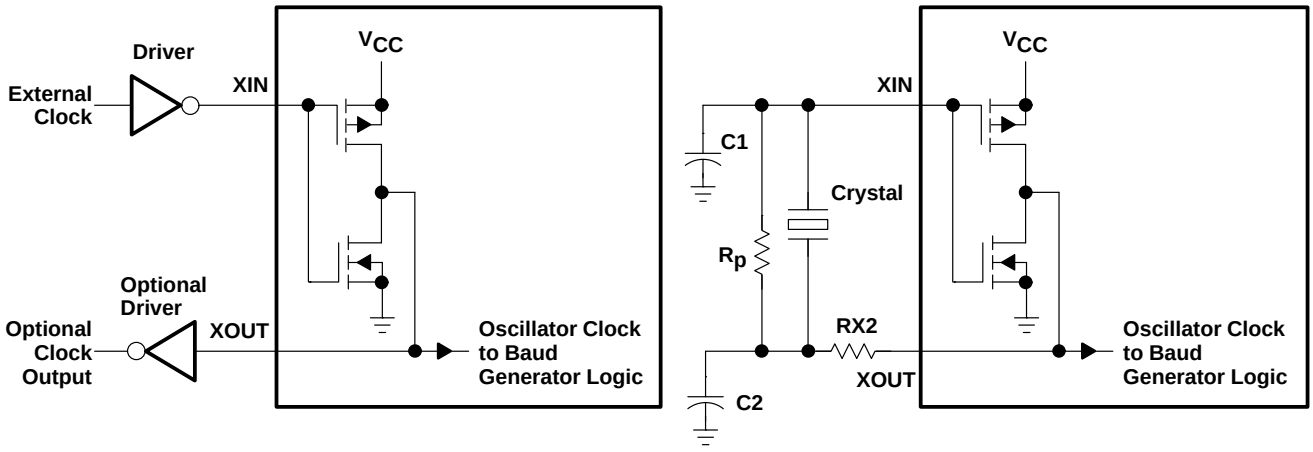
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 9. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	R_P	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 16. Typical Clock Circuits

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACEs RSR receives serial data from the SIN terminal. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. in the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

scratch register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is suppled by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and, when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the serial output (SOUT). In the TL16C450 mode, when the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

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